

Encapsulated Electronic Component And Production Method10/523875
DT01 Rec'd PCT 07 FEB 2005

The present invention concerns an encapsulated component in which there is a gap between a carrier substrate and the active surface of a chip, in particular a component
5 working with acoustic waves that contains a carrier substrate and a chip which is located on the top side of the carrier substrate, and is electrically and mechanically connected with it by means of bumps or other electrically conductive connections.

The chip is mounted on a substrate, for example on a piezoelectric substrate in the
10 case of an acoustic component, with the surface of the chip that faces the carrier substrate, referred to hereinafter as the underside, carrying electrically conductive structures, for example resonators that work with acoustic surface waves or volume waves.

A variety of methods have already been suggested for simple encapsulation of the
15 components to protect the sensitive conductive structures on the chip from environmental influences.

It is possible, for example, to seal the space between the chip edge and the carrier substrate with an underfiller and to sputter a metal layer onto the component. The
20 disadvantage of this method is that that the conductive structures (in particular acoustic converters) on the chip must be protected from the underfiller, for example with a plastic cap, and expensive processing steps are needed for this.

It was proposed in DE 198 06 818 A, for example, that the components be soldered onto a carrier in a flip chip arrangement and then be covered with a film, for example laminate film, which seals the components tightly with the carrier between the components.

In additional variants of such film coverings of components, it is also proposed that these films be further sealed hermetically by applying a metal layer over the film, and that this metallization be thickened for example by electroplating. In this case freestanding bumps are involved, which are not supported by a filling compound. Because the mechanical connection between the carrier substrate and the chip comes about exclusively through the laminate film and the bumps, the bumps in particular must endure the shear and/or tension stresses that occur in the chip under mechanical effects.

In particular as a result of differing coefficients of expansion of the laminate film or seals and the bumps, under strong and abrupt temperature changes the bumps are exposed to mechanical strains that can result in cracks, breaks, and even in the bumps breaking off.

The object of the present invention is to prevent mechanical strains of the electrically conductive connections in a component of flip chip construction, in particular bump connections, under extreme thermal loads.

This problem is solved according to the present invention by a component as recited in claim 1. Advantageous embodiments of the invention and the method of producing the component may be found in additional claims.

5

The invention provides a chip with electrically conductive structures on a surface referred to below as the underside of the chip, and a carrier substrate that is electrically and mechanically connected to this chip. The carrier substrate has connecting surfaces on its top side for making contact with the chip. The one or more chips is/are mounted on a carrier substrate in flip chip construction with the help of electrically conductive connections, preferably soldered connections, in particular bump connections (bumps), with the connecting surfaces of the carrier substrate being electrically connected to the electrically conductive structures of the chip.

10

Between the carrier substrate and the active surface of the chip there is a gap.

15

To relieve the electrically conductive connections, there is a support element positioned on the top side of the carrier substrate, which encircles the chip without touching it. The support element is preferably formed by a closed frame located on the top side of the support substrate, which encircles the chip. Furthermore, the component according to the present invention includes a seal that surrounds the chip, and tightly seals at least the space between the chip and the support element, which encircles it. In so

20

doing, the seal is supported on the support element.

The carrier substrate of the component according to the present invention can include one or more dielectric layers, made for example of a plastic, in particular organic
5 plastic, silicon, silicon oxide or ceramic, in particular LTCC or HTCC ceramic (LTCC = low temperature cofired ceramic, HTCC = high temperature cofired ceramic).

The ceramic can be made advantageously as a non-shrink ceramic. This guarantees only a slight change in dimension when sintering, so that a geometry specified
10 in the green film remains largely intact during sintering, or at least undergoes only a slight dimensional loss in a reproducible manner due to sintering shrinkage. With LTCC ceramics it is possible to provide the green films with cost-effective metallization, the tolerance of which for the low sintering temperatures of the LTCC ceramic is ensured.

15 It is also possible, however, to design the carrier substrate as a PCB (printed circuit board) in the form of a single-layer or multi-layer circuit board on a plastic base.

The dielectric layers are separated from each other by metallization layers, with the top side and the underside of the carrier substrate also forming metallization layers,
20 which have at least connecting surfaces for making contact with the chip or external contacts for soldering the component onto a system carrier (such as a circuit board). The metallization layers contain for example electrical connecting conductors, signal through-

connectors or integrated circuit elements (selected from an inductance, a capacitance or a conductor), which are formed in a known manner by conductor strips or conductor surfaces. The metallization layers are connected with each other by means of through connections.

5

The chip in the component according to the present invention includes a carrier substrate that may contain one or more dielectric layers which are separated from each other by metallization layers, with the top side or the underside of the carrier substrate also representing a metallization layer. The structure of the metallization layers and their connection with each other are as described above. The substrate can contain, for example, one or more layers of plastic, silicon or silicon oxide. The chip side intended as the metallization layer can have at least passive, non-linear or active component structure, in particular a diode or a transistor.

15 The component according to the present invention can be, in particular, a component that works with acoustic waves, in which the chip includes a substrate with at least one piezoelectric layer, where one side of the chip (for example the underside of the chip) has at least one surface wave converter or one volume wave resonator.

20 The substrate can contain a plurality of dielectric layers and metallization layers, as described above.

The component according to the present invention can also be a MEMS component (MEMS = microelectromechanical system, MOEMS = micro-optoelectromechanical system) or a semiconductor component, in particular an integrated circuit based on the semiconductor.

5

The seal can be made of a dielectric material, in particular of a filling compound such as resin, Glob-Top, underfiller, glue, or a plastic, in particular an organic plastic, a metal solder, glass solder or laminate film.

10 The seal at least partially covers the side surfaces of the chip and the sections of the support element that encircles it, and can completely or partially fill the space between the side surfaces of the chip and of the support element.

In an advantageous embodiment, the seal is designed as a dielectric layer which
15 also covers the top side of the chip. The dielectric layer can be formed by a filling compound, for example resin or a plastic layer, in particular a layer of an organic plastic or a glass solder or by a laminate film.

The dielectric layer can be made up of one or more layers, which, for example,
20 realize various functions. It is advantageous if one of the aforementioned layers exhibits especially low moisture absorption or especially good impermeability to gas. Especially suitable for this are layers of an LCP material (liquid crystal polymer). It is useful,

especially in the case of a dielectric layer realized as a film, which adheres poorly to the carrier substrate or chip, to provide an additional bonding layer.

The top layer in the structure of the dielectric layer can be an additional layer that is particularly well suited for laser inscription. It is possible that one of the layers in the structure of the dielectric layer is also suitable for filling the intermediate spaces between the chips on a large-area carrier substrate (panel). This layer can be realized with a filling compound.

It is also possible for the aforementioned seal to be combined with one or more of the aforementioned dielectric layers.

It is possible for the dielectric layer to completely cover the support element and the chip, and to form a seal with the carrier substrate only outside of the support element. Between the dielectric layer and the top side of the carrier substrate, there is a cavity, in which both the chip and the support element encircling it are enclosed. The support element can be of a hermetically tight or a non-hermetically-tight material.

In another advantageous embodiment, the seal is in the form of a dielectric layer which completely covers the chip and seals it tightly with the support element, with the outside of the support element not being covered by the seal. Here the support element is correspondingly of a hermetically tight material, and can form a part of the sidewall of the

component according to the invention.

In the preferred method of producing a component according to the present invention, the large-area carrier substrate (panel), populated with a number of chips, is laminated at a comparatively high temperature with a plastic film, which is stretched over the chip and the support element encircling it as it cools.

If the component is not yet hermetically sealed in this state, the hermetic condition is produced by an additional layer. This requires that the hermetic layer, for example a Cu layer, be sealed together with the support element or with the carrier substrate in the area between the installation locations of the chips. For this reason, the dielectric layer is removed at these places.

It is also possible to have the hermetic layer sealed directly to the surface of the carrier substrate at the edge of the component in a (ring-shaped) closed strip, with several or all of the chips of the component being located inside this closed strip. In this case the hermetic layer lies on the support element between the chips, and the chips of the component are hermetically tightly encapsulated not individually, but collectively.

It is possible for the component according to the present invention to include a plurality of like or different chips with passive or active components, which are located on the top side of the carrier substrate and encapsulated in the same way.

It is possible for the component also to include one or more discrete components, selected, for example, from a capacitor, a resistor or a coil.

5 Various methods are used to produce the electrically conductive connections, in the form of bumps. The bumps can be produced on the connection surfaces in the conventional way, by electroplating, for example by depositing SnPb, SnAg, SnCu, SnAgCu or SnAu. The electroplating can be followed by remelting, which results in formation of the corresponding alloy.

10 It is also possible to produce the bumps in a conventional way by means of screen or template printing with soldering paste, and then carrying out a reflow process in which the bumps acquire their spherical geometry.

15 It is also possible to produce the bumps by directed stamping of cylinders of soldering foil over the through connections of the topmost layer of the carrier substrate.

20 Alternatively, the bumps can also be produced on the solderable metallizations on the underside of the chip. This can also be done for example by electroplating over the corresponding metallizations. A solder jet method is also possible. Also possible is template printing of solder deposits on the metallizations, followed by a remelting process. Because here too the wettability of the solderable metallizations makes the

structuring easier, a difference in the wettability of metallic structures can be used to structure the bumps on the chip or in the wafer state. For example, it is possible to passivate a large part of the metallization located on the chip (the underside of the chip), for example by producing an anodic oxide layer, which can also be covered with an applied mineral layer, for example a thin layer of silicon oxide or a thin layer of silicon nitride. The surfaces that are not covered by this passivation then remain wettable with solder, or specially wettable with solder by suitable additional layers, so-called under-bump metallizations - UBMs -, while the passivated surfaces of the metallization represent the solder resist mask.

The support element located on the carrier substrate surrounds an interior space, which represents and geometrically defines the location for receiving the chip.

The support element can reach to above the level of the lower or upper edge of the chip. It is also possible, however, for the support element to be lower than the lower edge of the chip.

As an elevated structure, the support element is made of plastic, solder or metal, and can be produced as an integrated unit together with other components or structures of the carrier substrate. A support element made of metal or having metallization has the advantage that the metallization produces good contact, adhesion and wetting to the seal or dielectric layer, so that hermetic sealing of the entire component, and in particular of

the conducting structures on the underside of the chip, is guaranteed. It is also possible, however, for the surface of the support element to have no metallization.

The support element can also be of a ceramic material or a plastic, preferably of a plastic with a very low water absorption capacity (for example highly filled plastic or liquid crystal polymer).

The support element can also be produced with or by means of solderable metallizations. First metallization is produced on the carrier substrate at the places intended for the support element, for example in a sputter process. The support element can then be produced by thickening this metallization by electroplating. A sequence of layers of titanium (for better adhesion) and copper can be produced. Sufficient thickness of this layer can be produced already by sputtering, for example 100 to 200 nm titanium and more than 6 μm copper. It is also possible, however, to produce a thin titanium/copper layer (0.1 to 2 μm copper) and then to thicken this by electroplating. Preferably, structuring of the support element occurs with the help of a photoresist mask by structured sputtering. The mask can also be designed so that it can remain on the support substrate during the galvanic thickening process.

It is possible for the support element to be provided in the form of an individual frame for every chip located on the top side of the carrier substrate. It is also possible for the support element to be formed as a frame from a solid block, with recesses for each

chip.

The use of the support element encircling the chip when encapsulating the component with the help of a seal has the advantage that mechanical forces acting on the electrically conductive connections, which occur in particular under thermal loading and can lead to cracks, are reduced by supporting the seal on the support element, which contributes to mechanical relief of the electrically conductive connections.

The problem that the invention seeks to solve, i.e., avoiding overload of the electrically conductive connections, is also solved by an additional component. A chip is proposed with electrically conductive structures on the underside of the chip, and a carrier substrate which has connecting areas on the surface, with the chip being mounted in flip chip construction on the carrier substrate by means of conductive connections, and with the connecting areas being electrically connected to the electrically conductive structures of the chip by means of electrically conductive connections. Located on the top side of the chip is a cover, in particular a composite of a dielectric layer and above it a metal layer, with this composite forming a sealed connection with the carrier substrate around the chip outside of the chip area. To relieve the electrically conductive connections (preferably bumps), the chip thickness in the component is chosen so that the forces occurring due to the thermal expansion of the aforementioned composite in the temperature range between -60°C und 85°C are a maximum of 2 Newtons per electrically conductive connection (per bump).

The inventors have found that a force of over 2 Newtons acting on an electrically conductive connection, in particular a bump, leads to bump cracks; this is avoided according to the invention only by a suitable choice of the thickness of the layer. With
5 common chip sizes and bump arrangements used with them, this normally requires a reduction in the thickness of the chip. With this advantageous embodiment of the component according to the present invention, the desired relief of the electrically conductive connections (bumps) is achieved without a support element, which saves the corresponding procedural step to place the support element on the carrier substrate.

10 In another advantageous variant embodiment of the present invention, it is proposed that a dielectric layer of polymer material with a modulus of elasticity of less 1 GPa than be used, or a thin film whose thickness is less than 20 μm . In the aforementioned materials, with changing temperatures the deformation of the electrically
15 conductive connection is minimized by the fact that the deformation does not occur in the solder or in the electrically conductive connections, but in large part in the dielectric layer or in the film.

20 Alternatively, it is possible to use a dielectric layer or a film that has a low coefficient of thermal expansion, or in which the coefficient of thermal expansion is reduced by mixing in an inorganic filler material. Advantageously, a dielectric layer with a coefficient of thermal expansion that corresponds to that of solder or of the material of

the electrically conductive connections is used. It is also possible for the thermal expansion coefficient of the material of the dielectric layer to be selected between $\alpha_{\text{bump}}/2$ and $2\alpha_{\text{bump}}$.

5 For structuring of such dielectric layers or films with filler materials to be possible, preferably particles whose diameter is smaller than 1 μm are used.

In another variant embodiment of the invention, a component is also proposed that contains a chip with electrically conductive structures on the underside of the chip and a
10 carrier substrate which has connecting areas on the surface, with the chip being mounted in flip chip arrangement on the carrier substrate by means of conductive connections, and with the connecting areas being electrically connected to the electrically conductive structures of the chip by means of electrically conductive connections. The component according to the invention also contains a support element located on the top side of the
15 carrier substrate in the form of a shrink frame, which encircles the chip and tightly encloses it. This preferred embodiment of the invention has the advantage that the shrink frame simultaneously supports the chip being encapsulated and seals it tightly together with the carrier substrate, so that in this case in principle no additional seal is necessary. If the shrink frame is not sufficiently gas-tight, the hermetic quality of the parts can be
20 produced by an additional hermetically tight layer, preferably by a metal layer.

The problem underlying the invention is also solved by a method having the

following steps:

- at least two chips carrying conductive structures are attached by means of electrically conductive connections in flip chip arrangement to a carrier substrate, which has on its surface connecting areas for electrical connection with the electrically conductive structures of the chip,

- the at least two chips are covered with a dielectric layer which lies on the top side of the chip and seals it together with the carrier substrate, so that in this way each of the at least two chips is individually encapsulated,

- the space between the at least two chips is filled with a filling compound.

It is possible to apply to the dielectric layer a metal layer that forms a composite with the dielectric layer, and then to apply the filling compound to the composite of the dielectric layer and the metal layer outside of the chip and to cure it if necessary. The carrier substrate can then be sawed apart, so that individual components result which include at least one of the aforementioned chips.

In this advantageous method of producing a component encapsulated according to the present invention, the relief of the electrically conductive connections is achieved with an external support element positioned over the composite and formed by the filling compound (through a lateral support function). Compared to the corresponding process step of applying a structured "internal" support element to the carrier substrate, this represents a simplification of the process.

In the following section the invention, and in particular the method of producing a component according to the invention, will be explained in greater detail on the basis of exemplary embodiments and the associated figures, which are schematic and therefore not true to scale.

Figure 1 shows a component encapsulated according to the present invention having a carrier substrate, a chip placed on it, a dielectric layer and a support element, in schematic cross section.

Figure 2 shows an advantageous embodiment of the component encapsulated according to the present invention with the support element made of a hermetically tight material, in schematic cross section.

Figures 3 and 4 show advantageous embodiments of the component encapsulated according to the present invention, in schematic cross section.

Figures 5a and 5b show a component according to the present invention with a filling compound between the encapsulated chips, in schematic cross section.

Figures 6a and 6b show a component according to the present invention with a thinned chip, in schematic cross section (in normal condition and at a substantially lower temperature).

Figure 6c shows an exemplary arrangement of the electrically conductive connections of the thinned chip in the component according to the present invention, in schematic cross section parallel to the chip surface.

Figures 7a through 7c show successive process steps in the encapsulation of the component according to the present invention, with a chip having sloping side surfaces and a solder frame.

5 Figure 1 shows a schematic cross section of a carrier substrate TS with a chip CH placed on it and a support element SE. The component includes the chip CH mounted on the carrier substrate TS in flip chip arrangement by means of electrically conductive connections BU, and a support element SE located on the top side of the carrier substrate, which encircles the chip.

10 In the component according to the present invention, the chip is not lying on the support element.

 The chip and the support element together are covered with a seal AB in the form
15 of a dielectric layer. In this exemplary embodiment a metal layer ME is additionally applied to the dielectric layer AB. The metal layer serves to shield the signal-carrying chip structures from electromagnetic interference and to produce the hermetic condition.

 In addition, the top side of the chip can be provided with continuous metallization,
20 or with a layer, for example an adhesion layer, which enables better adhesion of the dielectric layer AB.

The carrier substrate TS contains one or more dielectric layers, with layers of metallization ML being provided on its top side, underside and possibly between two dielectric layers. The top side of the carrier substrate has in particular connecting areas AF, which are electrically connected to the electrically conductive structures of the chip.

5 The underside of the carrier substrate has in particular external contacts AK (for example SMD-capable contacts; SMD = surface-mounted device). The external contacts are connected with the connecting areas and with the metallization layers ME, if any, by means of through connections DK. The metallization layers of the multi-layer carrier substrate can contain integrated circuit elements formed by conductor strips and metal
10 areas, selected for example from a capacitance, an inductance, a conductor or a segment of a conductor.

The chip CH contains for example a piezoelectric substrate, whose surface (underside) bears metallizations of a surface wave component and/or at least one FBAR
15 (thin film bulk acoustic wave resonator), referred to hereinafter as component structures. The chip can also be a multi-layer substrate with integrated circuit elements. It is possible for the top side of the chip to be metallized, for example by a Cu sputter layer that is thickened by electroplating.

20 The circuit elements integrated into the carrier substrate, by themselves or together with the component structures or circuit elements arranged on the chip or in the chip, can form at least a part of the following circuits: a high frequency switch, a matching circuit,

an antenna switch, a diode switch, a transistor switch, a high pass filter, a low pass filter, a band-pass filter, a band-stop filter, a power amplifier, a preamplifier, an LNA, a diplexer, a duplexer, a coupler, a directional coupler, a storage element, a balun, a mixer or an oscillator.

5

The expansion coefficient of the support element α_{frame} is preferably approximately the same as the expansion coefficient of the electrically conductive connections α_{bump} , and is smaller than the expansion coefficient of the cover α_{cover} . The height of the support element over the surface of the carrier substrate can be for example approximately equal to or greater than the height of the electrically conductive connection or the bump height. It makes sense to choose the height of the support element h so that it is connected with the interval g between the top side of the carrier substrate and the contact point of the film on the chip, as follows:

10

15

$$h \approx g \cdot (\alpha_{bump} - \alpha_{cover}) / (\alpha_{frame} - \alpha_{cover}).$$

It is also possible for the height of the support element in the entire specified temperature range (e.g., -60°C ... +85°C) to be lower than the height of the electrically conductive connection (or bump height) at the same temperature. In this case the width of the support element can be selected so that the inner edge of the support element lies outside the area covered by the chip, as shown in Figure 1, or extends under the chip.

20

It is also possible for the height of the support element to be greater than, equal to or smaller than the distance between the top of the chip (or the underside of the chip) and the top of the carrier substrate.

5 The support element SE preferably follows the external shape of the chip CH, and is therefore in particular rectangular in shape (in the top view).

 The support element can be made of metal, solder, ceramic or plastic. The support element made of plastic can be produced for example from a photosensitive resist, or can
10 be structured from another layer with the help of a photolithograph or a laser. The support element of metal can be produced by screen printing or by electroplating.

 Because in this example hermetic encapsulation of the chip in the component is achieved by having both the dielectric layer of the seal AB and the metal layer ME sealed
15 together with the carrier substrate outside of the support element, it is possible for the support element to be made of a material that is not hermetically tight.

 The support element can be provided on one side with an adhesion layer, glass solder or a solderable layer, for example of metal solder, so that the support element can
20 be attached to the top side of the carrier substrate.

It is possible for the support element to be firmly connected with the carrier

substrate or to form an element of the carrier substrate, in which case the support element and the carrier substrate can be of the same material and can be produced for example at the same time.

5 The bumps can be produced by electroplating, by a solder jet process (e.g., laser bumping), by stud bumping or by printing. Alternatively, an anisotropically conductive adhesive can also be employed, which is applied for example to the top side of the carrier substrate. In this case, signal-bearing structures (on the chip side) may need to be protected, for example by a protective cap or a protective layer.

10 Figure 2 shows another advantageous embodiment of the component according to the present invention. In contrast to the exemplary embodiment presented in Figure 1, the dielectric layer AB does not form a seal with the carrier substrate TS, but only with the support element SE. In so doing, the dielectric layer AB covers only part of the support
15 element, so that the metal layer ME forms a seal with the area of the support element not covered by the dielectric layer. Because the support element SE here represents part of the side wall of the component, in this case hermetic encapsulation of the chip in the component is only guaranteed if the support element is made of a hermetically tight material (e.g., ceramic, metal or solder).

20 The exemplary embodiment shown in Figure 3 corresponds to Figure 2, while the support element SE here can be part of the carrier substrate TS. In this example, the

height of the support element can be approximately equal to the distance between the top of the chip and the top of the carrier substrate. It is also possible for the height of the support element to be greater or less than the distance between the top of the chip and the top of the carrier substrate.

5

It is possible for the seal AB formed as a dielectric layer to be continuous, and in particular to completely cover the surface of the support element. This has the benefit that such a layer is especially simple to apply. If the dielectric layer at the same time ensures a hermetic seal, the metal layer ME can be dispensed with.

10

In the exemplary embodiment shown in Figure 4, the space between the chip CH and the support element SE is sealed with the seal AB. In this case the seal covers only the adjoining or directly opposing edge areas on the top of the chip and the support element.

15

The seal can be of glass solder or filling compound (e.g., glue or resin). In this case it makes sense to shield the chip, to apply a metal layer ME in such a way that it covers the top side of the chip, the seal, and the surface of the support element not covered by the seal.

20

It is possible for the top of the chip and the surface of the support element to be metallized even before the seal is applied, and for the seal to be of solder. In this case it is

possible to dispense with the continuous metal layer, which covers in particular the seal.

Figure 5a shows an advantageous embodiment of the invention, without a support element. The chip CH is positioned on a large-area carrier substrate TS (panel), and as indicated in the figure is surrounded by additional (like or differing) chips. Each chip
5 belongs for example to an installation location on the panel. The chips are encapsulated in the same manner with a dielectric layer AB. Because the dielectric layer AB generally does not permit a hermetic seal, the hermetic state is produced by an additional hermetic layer ME. To that end the hermetic layer, in particular a metal layer, for example a Cu
10 layer, which forms a composite with the dielectric layer, is supposed to form a seal in the area between the installation locations. For this reason, the dielectric layer is removed at these places.

The relief of the electrically conductive connections is achieved here by having the
15 spaces between the encapsulated chips at least partially filled with a filling compound VM (e.g., resin or Glob-Top) having a suitable expansion coefficient. The material and the height of this filling are selected so that the higher expansion coefficient of the dielectric layer AB (compared to the expansion coefficient of the electrically conductive connections) is compensated for, and so that the expansion coefficient of the composite of
20 the filling compound, the dielectric layer and the metal layer ME in the area between the top side of the carrier substrate and the bottom edge of the chip is matched to the coefficients of expansion of the electrically conductive connections. After the filling

compound VM has cured, the large-area carrier substrate with the chips positioned on it at corresponding individual installation locations can be separated into individual components, and in particular can be sawed apart. The separate components can contain one chip or a plurality of chips.

5

In the exemplary embodiment shown in Figure 5b, the chips are encapsulated as described above and arranged on the large-area carrier substrate TS, the carrier substrate later being separated, for example sawed, into individual components. In Figure 5b, the relief of the electrically conductive connections is achieved as in Figure 5a by the filling compound VM and in addition by the support element SE.

10

In a preferred exemplary embodiment the filling compound is topped up to the top edge of the chip, in order to obtain a block-shaped component (after the separation by sawing), which can easily be placed during the later SMD installation.

15

Figures 6a and 6b show another advantageous embodiment of the present invention.

During an abrupt temperature change, the chip, the carrier substrate, the dielectric layer, the metal layer and the electrically conductive connections (e.g. bumps) undergo varying expansions due to the different, and in some cases also directionally dependent coefficients of thermal expansion. The electrically conductive connections (bumps) in

20

particular must endure the occurring mechanical stresses, in particular the shear stresses. The simulation of the component according to the present invention shows that cracks are caused in a bump with a diameter of about 180 μm starting at a shear force of about 2 N acting on it, which can result in impairment of the function of the component and even in
5 the bump breaking off of the UBM (external electrodes AE on the side of the chip and connecting areas AF on the side of the carrier substrate).

It is possible to increase the tolerance to temperature changes of the component according to the present invention, either by selecting such a small chip thickness or by
10 reducing it by thinning the chip to such a degree that the force needed to bend the chip CH in the entire specified temperature range (e.g., -60°C to $+85^{\circ}\text{C}$) is significantly smaller than the force sufficient for the electrically conductive connections BU to break off of the UBM or the connecting area AF, or the force sufficient to form cracks in the bumps (e.g., 2 N per bump). The exact value of the chip thickness depends on the ratio of the
15 coefficients of expansion of the dielectric layer AB and the metal layer ME, of the chip CH, the electrically conductive connections BU and of the carrier substrate TS, and on geometric factors (e.g. chip size, size of the electrically conductive connections or the distance between the electrically conductive connections), and can be ascertained by simulation.

20 In an advantageous exemplary embodiment shown in Figure 6c, the chip CH1 of lithium tantalate (with a directionally-dependent coefficient of thermal expansion of about

7.0 – 14.3 ppm/K), width $a = 1.2$ mm and length $b = 1.8$ mm, is connected to a carrier substrate not shown here having a width of 2 mm and a length of 2.5 mm (with the coefficient of thermal expansion of 6.3 ppm/K) by means of six bumps BU1 of SnAg(3.5)Cu(0.8) (with a coefficient of thermal expansion of 20.0 ppm) having a height of 50 μm .

The bumps are arranged at equal intervals in two parallel rows of 3 bumps each along the longer edge of the chip. The spacing $L1$ of the bumps in a row is 800 μm . The space $L2$ between the rows is 900 μm . The covering over the chip consists of a film 50 μm thick (with a coefficient of thermal expansion of 130.0 ppm/K in the relevant temperature range), and a 20 μm thick Cu layer over that which has a expansion coefficient of 7.1 ppm/K. Numerical simulations of the expansion behavior for the relevant temperature range have shown that the resulting force occurring per bump at a chip thickness of < 250 μm is under 2 Newtons.

Thinning the chip

In an advantageous variant of the present invention, the chip is thinned in order to achieve relief of the electrically conductive connections. It is possible to use a DBG process (dicing before grinding) for this. In this process the not-yet-separated chips are thinned in the wafer stage, i.e., before being soldered to the carrier substrate. First one surface of the wafer (here called the underside) is sawed into along the intended sawing

line or structured in some other way. The depth of the saw cut or structure indentation is less than the thickness of the wafer, and preferably equal to or somewhat greater than the remaining chip thickness achieved after the thinning. Next, part of the material on the top side of the wafer is removed, while at the same time the chips are separated on the sawed
5 and thinned wafer.

The chips can also be thinned after being soldered on, in order to achieve the purpose indicated above. The chip, which has a thickness of around 250 μm or more, can be thinned to a thickness of 50 to 100 μm . Especially well suited for the thinning is a
10 particle jet with aluminum oxide particles having a diameter of $< 50 \mu\text{m}$. It is also possible to grind the chip down. Before the processing with the particle jet, the areas on which cutting is to be prevented can be covered with a soft resist mask, for example a photosensitive resist mask. It is also possible, however, simultaneously with the thinning of the chip, to remove areas of the carrier substrate or even to sever it completely by
15 means of the jet process. In this case it may be necessary to cover the chip also beforehand with a mask.

In an advantageous variant of the present invention it is possible to pre-thin the not-yet-separated chips on the wafer, as indicated above, and to thin them further after
20 they are soldered on using a jet process (such as sand blasting), in order in particular to achieve rounding of the edges, which is desirable for example when applying a film cover.

Figure 7 shows an alternative embodiment of the present invention. Here a support element SE in the form of a solder frame is produced on the carrier substrate before the chip CH is placed in position. To this end, a metallization (reference symbol AE) similar to an under-bump metallization (UBM) is produced on the carrier substrate at the places intended for the solder frame. The solder frame can then be applied by printing it on, by thickening the USM by electroplating, or also as a frame-shaped piece of soldering foil. In this version the side edges of the chip are sloped in such a way that the chip is tapered toward the surface with the electrically conductive structures, which may be applied in the later processing step (called the underside of the chip). It is then metallized on the sloping side surfaces. Preferably, the metallization of the side surfaces takes place in the same process step as the production of the electrically conductive structures and the UBM on the underside of the chip.

In addition, the side surface of the chip can be vapor-plated for example with a Ti/Cu layer, so that the conductive structures on the underside of the chip can be protected with a photoresist.

In addition to the electrically conductive structures, the underside of the chip has external electrodes AE, a contact metallization KM, and positioned on the lower edge of the chip insulating, non-wetting structures IS. The insulating structures prevent a short circuit between the external electrodes AE and the contact metallization KM. They can be structured of plastic or solder resist, or can be produced by passivating the metal

structures. Where there is sufficient distance between the external electrodes AE and the contact metallization KM, the insulating layer IS can be dispensed with.

The top side of the chip can be additionally provided with a metal layer for
5 shielding purposes.

In this exemplary embodiment the electrically conductive connections (bumps) are located on the top side of the carrier substrate TS before the chip is placed in position. The chip can then be placed on the carrier substrate (see Figure 7b) in such a way that it is
10 positioned with the sloping side edges over the solder frame and is supported from beneath by the electrically conductive connections (bumps). The frame height and the height of the electrically conductive connection (bump height) are selected so that the collapse of the solder or bump during the soldering causes the chip to be brought into contact with the solder frame. During the soldering a soldered connection of the solder
15 frame to the contact metallizations KM at the side edges of the chip comes about (reference symbols AB, SE in Figure 7c), with the soldered connection serving as a hermetic seal between the chip and the carrier substrate and with the seal AB being formed by the solder frame after the soldering.

20 It is possible, instead of the chip with the sloping side surfaces, to use a chip whose side surfaces have at least one step, so that in cross section the chip is approximately T-shaped. In that case the (partial) metallization of the side surfaces of the

chip can take place on the step and in the same process step as the production of the electrically conductive structures and the UBM on the underside of the chip.

In another exemplary embodiment of the component according to the present invention, a support element in the form of a frame exhibits shrinkage behavior, so that after temperature exposure the frame lies tightly against the chip. In this case the further sealing can be dispensed with and the component can be closed directly by a hermetically tight layer, in particular a metal layer (for example a Cu sputter layer that is thickened by electroplating), with the hermetically tight layer covering the top side of the chip and the shrink frame and forming a seal with the carrier substrate. The frame can be provided on one side with a solderable layer or with an adhesive layer, which connects the frame with the carrier substrate.

The invention has been presented on the basis of only a few important exemplary embodiments, but is not limited to these. Additional variants of the component according to the present invention and of the method of producing it consist in particular in other geometric configurations, other materials to be used, or in the employment of analogous processes with which the same effects can be achieved. The seal between the chip and the support element or carrier substrate, and devices or measures with which the relief of the electrically conductive connections according to the invention can be achieved remain essential, however.

With the method according to the present invention, preferably a plurality of chips can be placed simultaneously on a carrier substrate of appropriately large size and can be attached and encapsulated. The carrier substrate can then be severed between individual chips, in order to separate individual components or groups of components wired together
5 into modules. The severing and separating can be done with a jet process or by sawing. Surface layers, and in particular metallizations that are to be severed, can be structured in advance if appropriate and can then be removed by wet chemical means or by plasma etching.